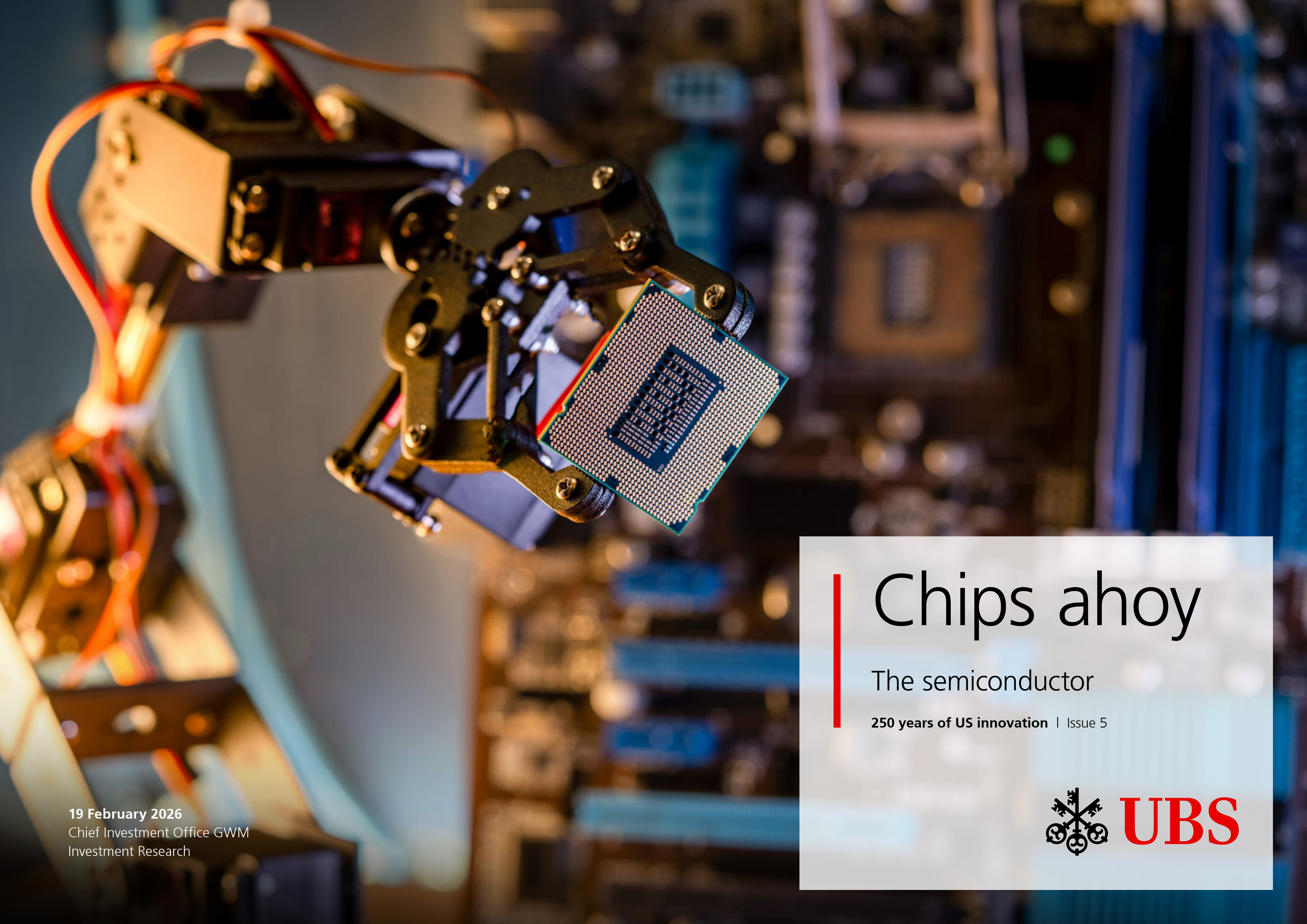

Chips ahoy

The semiconductor

250 years of US innovation | Issue 5

UBS

19 February 2026
Chief Investment Office GWM
Investment Research

Chips ahoy

For many, the mythology of the information technology sector's rise begins in a modest garage somewhere in the neighborhood of Menlo Park or Santa Clara, California. But that's not quite how it all started.

Before Silicon Valley became today's hub, or central processing unit, for technology, there were numerous foundational discoveries dotting the US landscape along the way. For example, in the 1940s and 1950s, scientists at Bell Labs—a subsidiary of the telecommunications giant AT&T headquartered in central New Jersey—spearheaded much of today's research into early transistors. A few years later and thousands of miles to the south in Dallas, Texas, researchers at a much smaller firm, originally founded for oil exploration, developed the first commercially viable silicon-based transistor. That breakthrough paved the way for that small firm to become one of the early titans of the microchip: Texas Instruments. Then, back on the Pacific Coast in Palo Alto, California, the first commercially viable integrated circuit was born at a company called Fairchild Semiconductor. Robert Noyce and Gordon Moore resigned from Fairchild to found Intel Corporation in 1968.

The early semiconductor industry was highly reliant on federal government policy and financial support, especially for defense and aerospace, to achieve scale and ultimately realize resounding commercial success. Government assistance of transformational technologies is nothing new. It played a large role in the building of the transcontinental railroad (Issue 1, 27 October 2025) and the viability of commercial aviation (Issue 3, 17 December 2025). Private-sector sales of semiconductors dominate today, but the industry benefited from government procurement to provide a kickstart.

After having lost substantial market share to Japanese producers of memory chips in the 1980s, the US sought and achieved market access concessions from Japan in 1986 in exchange for export restraints. The US government is once again actively working to revive some of the early dynamism of semiconductor production, exemplified by initiatives like the 2022 Creating Helpful Incentives to Produce Semiconductors (CHIPS) for America Act. International competition to stay ahead in the artificial intelligence (AI) arms race, the harsh realities of supply bottlenecks during COVID-19, and the susceptibility to losing access to the critical minerals needed to manufacture semiconductors are all factors driving today's policy decisions.

Ahoy, the AI race is on, helping to spur additional spending on semiconductor research, manufacturing, and design. The US semiconductor industry remains at the cutting edge of chip design, but it lags in manufacturing capabilities. While there is much anticipation about the future for semiconductors, nearly 70 years after their initial discovery, there is also no room for complacency.

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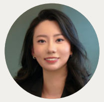
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Infographic

The speed at which technology has grown is staggering, and the invention of the microchip played a pivotal role in this evolution. The domino effect that began with the creation of the first transistor has led to the modern adoption of AI, and comparing the power of something as ubiquitous as today's common smartphone to the computer behind the Apollo missions shows how far we've come in just a few short decades. The science behind semiconductors is equally as ever evolving, and the industry's scale has reached unprecedented levels, making waves across markets and innovation.

Standard computational benchmark to compare quantum computer and supercomputer speed

Today's fastest supercomputers
10,000,000,000,000tr years

Google's Willow (Quantum chip)
<5 minutes

Size of a microchip if the transistor size stayed constant from 1971

Size of microchip (1971)
10,000 nanometers

Size of microchip (2025)
3,824,900,000 nanometers

	1961	1971	1994	2025
Number of transistors	4	2,300	1,350,000	16.6 bn
CPU speed (kilohertz)	100-300	740	150,000	4,300,000
Price per chip (2025 USD)	335	480	3,466	500

	Computer used for Apollo missions to the moon	Modern smart phones processing power
RAM	4 kB	12.6mn kB
ROM	73.7 kB	268.4mn kB

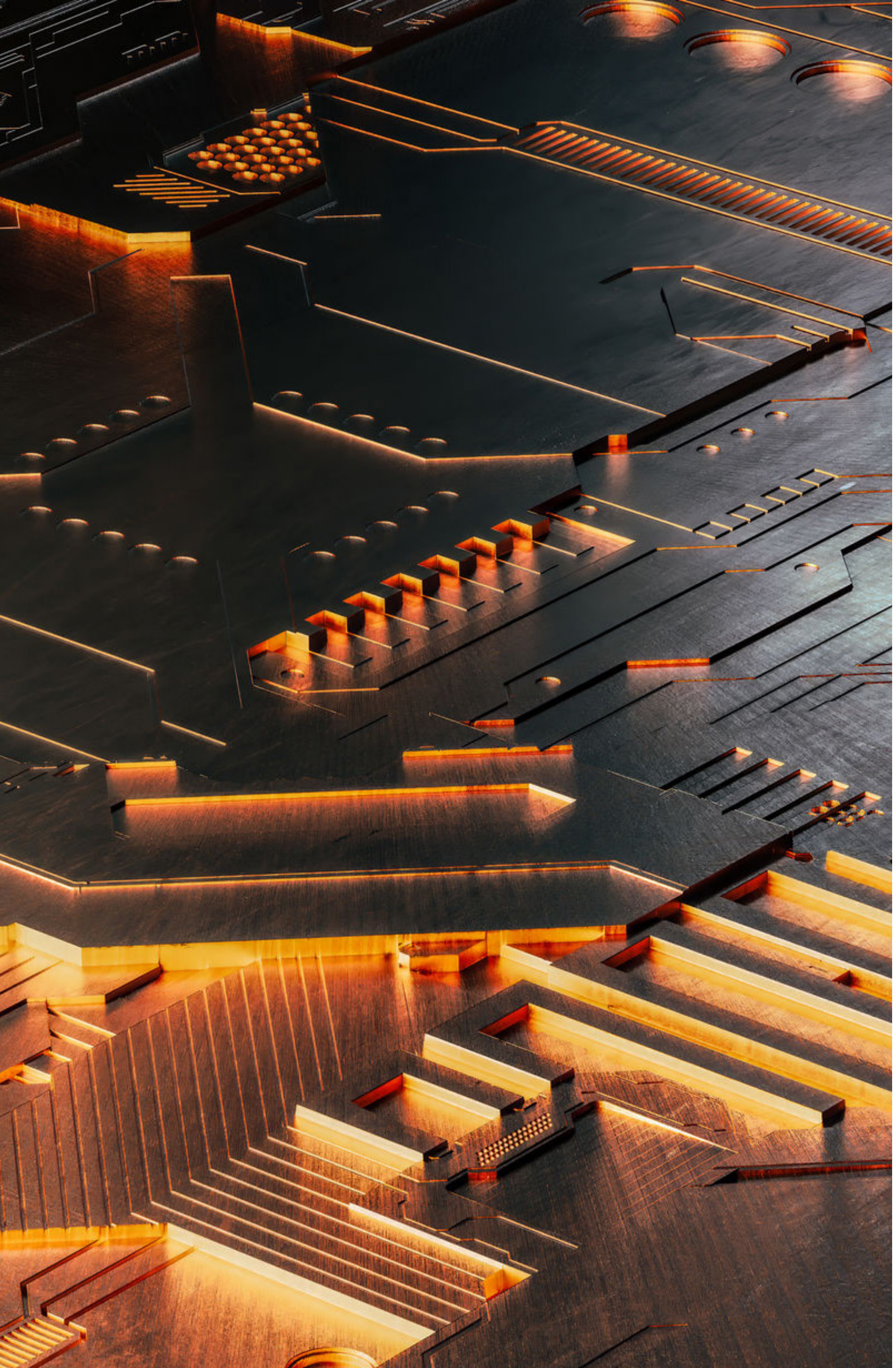
Top US exports in 2024 (in USD)

Semiconductors	Cars	Natural gas	Aircraft	Refined oil
57bn	61bn	62.6bn	123.3bn	123.4bn

Number of elements used to make a semiconductor

1980s	1990s	2000s	2010s
17	21	62	66

Source: Semiconductor Industry Association, ASML, Google, Lam Research, Intel, MIPS, UBS as of 10 February 2026



The history lesson

The microchip, or integrated circuit (IC), forms the backbone of modern electronics. Its invention and subsequent evolution have fundamentally transformed industries, economies, and daily life—enabling technologies ranging from smartphones to supercomputers.

A pivotal milestone in microchip history was the invention of the transistor at Bell Labs in 1947. Transistors, which amplify or switch electrical signals, are the essential building blocks of integrated circuits. In the 1950s, transistors were large and cumbersome, primarily used in radios and room-sized computers. In April 1954, a Texas Instruments (TI) team led by Gordon Teal developed and commercialized the first silicon transistor, whose high-temperature performance made silicon transistors superior to earlier germanium-based transistors for military and industrial applications. In 1957, Jay Lathrop advanced the field by developing photolithography—a process utilizing light to etch intricate patterns onto semiconductor materials. By inverting a microscope lens to shrink these patterns, Lathrop enabled the miniaturization of transistors, paving the way for compact integrated circuits.

The late 1950s marked the true beginning of the microchip era, as two engineers independently developed the first integrated circuits. In 1958, Jack Kilby at TI successfully integrated all components of an electronic circuit onto a single piece of semiconductor material, creating the first microchip. In 1959, Robert Noyce at Fairchild Semiconductor filed a patent for the first practical microchip using silicon—a more effective material for mass production—thus laying the groundwork for the modern microchip. These inventions accelerated the rapid technological progress in the semiconductor industry.

The first microchips contained just four transistors, were priced at approximately USD 31 in 1960 (equivalent to roughly USD 330 in 2025 dollars) and were deployed in military and aerospace applications (see Fig. 1). Their compact size, reliability, and efficiency made them ideal for space missions. For example, the US Air Force utilized them in its Minuteman II missile guidance systems, and the National Aeronautics and Space Administration incorporated them into the Apollo projects.

Advancements in lithography have enabled the exponential progress described by Moore's Law—named after Gordon Moore, co-founder of Intel—which predicts that the number of transistors on a microchip doubles every two years (see Fig. 2). This principle has become the industry standard for chip design, resulting in dramatic increases in computing power and significant reductions in cost. By the early 1970s, substantial investment by the US Department of Defense facilitated mass production of microchips, which drove the unit cost of these earlier models down to USD 1.25. As Fred Kaplan, author of "1959: The Year Everything Changed" notes, "It was the government that created the large demand that facilitated mass production of the microchip." Over more than five decades, ongoing breakthroughs in lithographic techniques have driven aggressive scaling of process node dimensions, shrinking feature sizes from thousands of nanometers in the 1970s to just a few nanometers today.

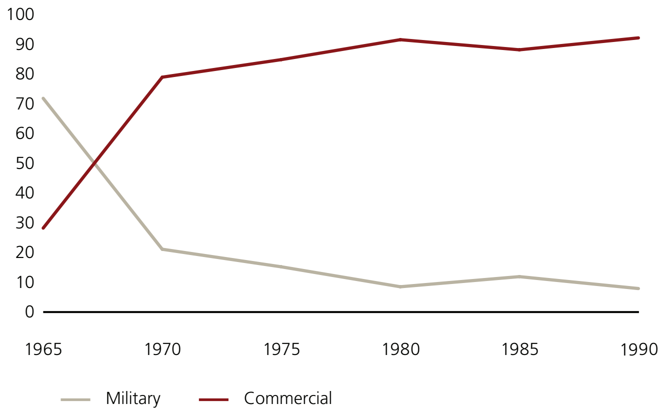
Up to this point, microchips were designed to perform single, specific computing tasks. This changed in 1971 with the release of the Intel 4004—one of the first commercially available microprocessors. For the first time, the functions of an entire computer central processing unit were integrated onto a single silicon chip. This innovation marked the advent of widespread logic chip adoption in consumer electronics and signaled the onset of the digital revolution. As a result, products became smaller, faster, and more affordable. Early applications included calculators, hearing aids, and, eventually, the first personal computers.

During the same era, memory chips emerged as a solution for data storage. The first commercially available random access memory (RAM) and read-only memory (ROM) chips appeared

Figure 1

US military facilitated commercial adoption of semiconductor

US integrated circuit sales as a share of total, in %

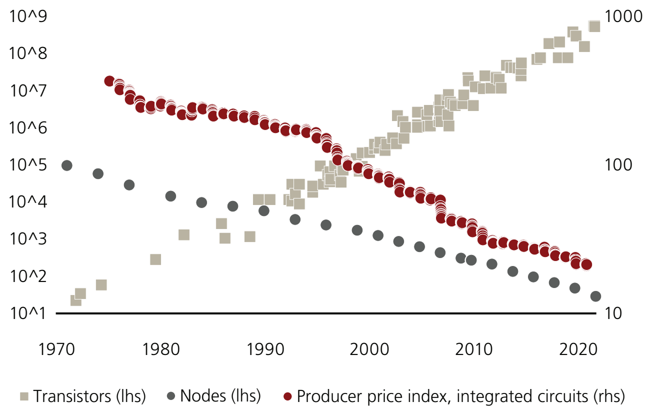


Source: John A. Alic, Lewis M. Branscomb, Harvey Brooks, Ashton B. Carter, and Gerald L. Epstein, "Beyond Spinoff: Military and Commercial Technologies in a Changing World" (1992), UBS as of 8 February 2026

Figure 2

A doubling of transistors every two years

Number of transistors and size of nodes (in nm) versus producer price index for integrated circuits, log scale



Note: Original transistor data up to the year 2010 collected and plotted by M. Horowitz, et al. New plot and data collected for 2010-2021 by K. Rupp. Source: K. Rupp, "Microprocessor Trend Data" (2022) available under a Creative Commons Attribution 4.0 International Public License, St. Louis Federal Reserve, UBS estimates, UBS as of 8 February 2026 in the 1960s and 1970s, allowing devices to execute software and retain essential instructions. As technology advanced, memory chips increased in both capacity and speed.

The 1970s and early 1980s proved to be a period of rapid productivity growth for the emerging semiconductor industry sector. According to the Bureau of Labor Statistics, output per hour advanced 13% on an annualized basis from 1972 to 1986 even as overall US productivity grew only 2% (see Fig. 3). Employment in the industry grew steadily, but output grew more than twice as fast. Improved manufacturing processes boosted production volumes, which enabled chip prices to decline and yielded far broader adoption across a range of new applications.

International competition in the semiconductor industry emerged rapidly. By the late 1970s, Japan had become a major producer of semiconductors. According to Laura D'Andrea Tyson in "Who's bashing whom?: Trade conflict in high-technology industries" (1992), US market share of dynamic random-access memory (DRAM) chips plummeted from 70% to 20% between 1978 and 1986 as the Japanese market share jumped from under 30% to around 75%.

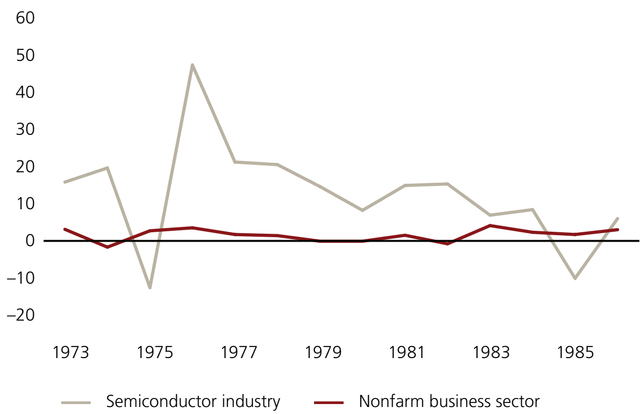
In 1986, the two countries signed the US-Japan Semiconductor Agreement, establishing a government-supported framework that effectively fixed microchip prices and limited Japan's exports of DRAM chips to the US. Following the agreement, the US maintained its leadership in microchip manufacturing relative to global competitors for more than two decades at the cost of higher prices for semiconductor purchasers. However, the US eventually began to shift its strategic focus toward design, innovation, and research and development (R&D), which was accompanied by reduced capital investment and increased outsourcing of chip manufacturing to overseas foundries.

Notably over the past three decades, Taiwan has also been strategically positioning the semiconductor industry as a cornerstone of its national competitiveness. Through targeted industrial policy, including significant investments in R&D and the recruitment of US-trained Taiwanese engineers and managers, Taiwan established the Hsinchu Science Park in the 1980s. This initiative has since evolved into a global powerhouse for chip manufacturing.

Figure 3

Rapid early advances in semiconductor productivity

Annual change in output per hour for the semiconductor industry and nonfarm business sector, in %

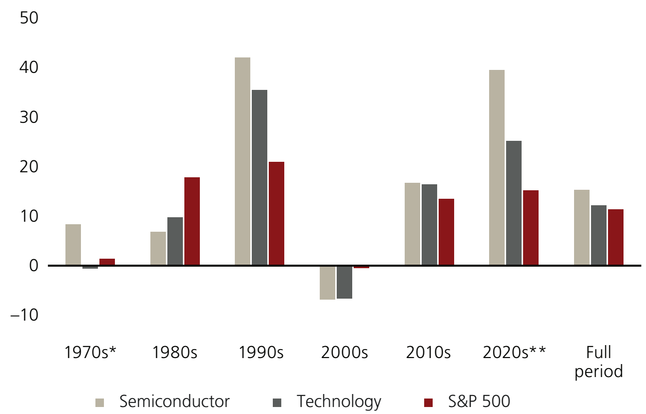


Source: Mark Scott Sieling, "Monthly Labor Review: Semiconductor productivity gains linked to multiple innovations" (1988), Bureau of Labor Statistics, UBS as of 9 February 2026

Figure 4

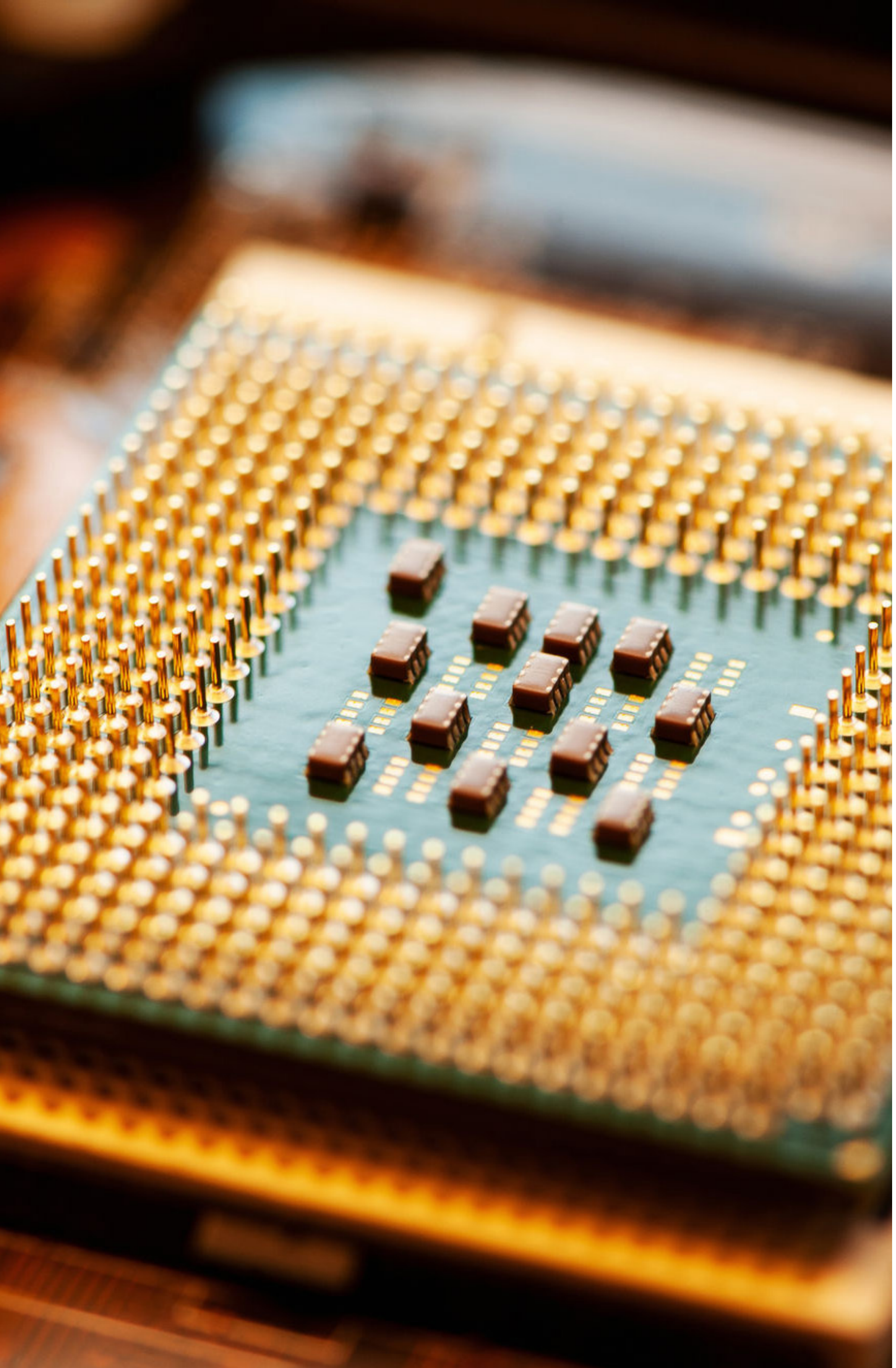
Semiconductor stocks outperformed over the long term

Annualized total return by decade for the semiconductor industry, the technology sector and the overall S&P 500, in %



Note: *1970s includes the years 1973-79. **2020s includes the years 2020-25.
Source: Refinitiv Datastream, UBS as of 9 February 2026

Semiconductor stocks outperformed the technology sector and the broad S&P 500 in the early years but then underperformed in the late 1980s as DRAM prices collapsed and growing competition from Japanese companies undercut margins and prompted rising trade tensions (see Fig. 4). The production of increasingly complex microprocessors required greater capital investment than earlier fabrication methods, pressuring free cash flow. However, this underperformance proved short-lived, as semiconductor companies leapt ahead in the 1990s and have remained at the forefront ever since.



A modern view

Today, specialized chips are engineered to address increasingly diverse requirements. Graphics processing units (GPUs), originally designed for rendering video game graphics, are now critical for artificial intelligence (AI) applications owing to their ability to perform millions of parallel calculations—ideal for deep learning and large-scale data analysis. Neural processing units (NPUs), optimized for embedded AI, enable rapid on-device processing in smartphones, voice assistants, and autonomous vehicles.

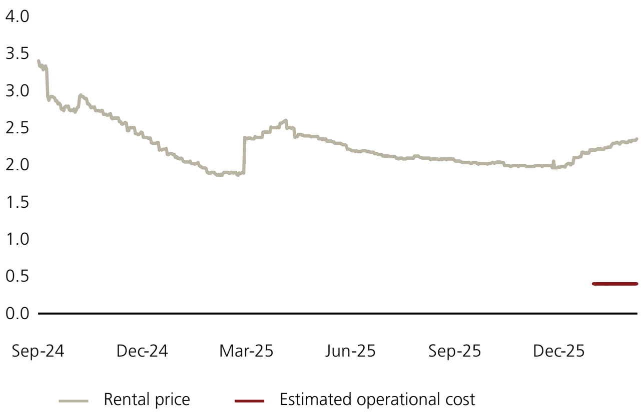
Microchip innovation has powered a sweeping digital transformation, embedding computation into daily life and connecting billions through personal computing, mobile devices, and the internet. This wave has democratized access to information, education, and services, reshaped communication and commerce, and catalyzed health care advances. It has also turbocharged automation and workforce productivity, lifting economic growth and tightening global connectivity. This same momentum brings new complexity, as data privacy and cybersecurity emerge as central challenges in a world that runs on silicon.

GPUs have become the backbone of modern AI compute. They are designed to handle thousands of tasks simultaneously, a concept known as parallelism. This makes them uniquely suited for the large-scale matrix operations required in machine and deep learning, where massive computational power is needed. Modern GPUs feature thousands of stream processing cores, high-bandwidth memory (HBM), and advanced interconnects, supporting rapid training and inference of complex neural networks. For data center operators, renting out high-end GPUs often yields a significant margin, as the operational cost is around 40 cents per GPU per hour compared to the much higher rental revenue (see Fig. 5).

Figure 5

GPU hourly rental price exceeds estimated operational cost

Silicon Data H100 Rental Price Index, in USD per GPU per hour



Source: Bloomberg, UBS as of 9 February 2026

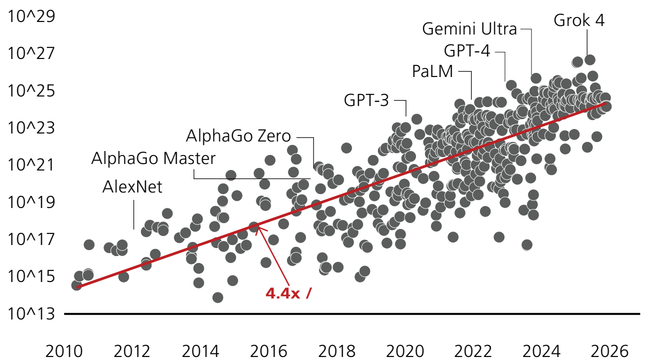
Importantly, GPUs are essential for training frontier AI models (such as OpenAI's ChatGPT, xAI's Grok, Anthropic's Claude). As such, their scalability and support for AI-optimized frameworks have made GPUs indispensable for data centers and cloud AI workloads, driving exponential growth in model size and performance (see Fig. 6).

To optimize the efficiency of modern high-performance computing, the industry has been shifting from traditional chip placement to advanced packaging techniques that minimize the distance between compute, memory, and networking components. Chip-on-Wafer-on-Substrate (CoWoS) serves as the current foundational 2.5D packaging technology for AI accelerators, utilizing a silicon layer, or interposer, to bridge the gap between logic and memory. By mounting high-performance processors and HBM stacks onto this intermediate silicon layer, CoWoS enables thousands of dense interconnections that far exceed the data rates of a standard circuit board. This architecture has become the gold standard for modern GPUs, as it provides the massive memory bandwidth required to feed large language models while keeping power consumption low through shortened electrical paths.

Figure 6

The training compute of notable AI models has been doubling roughly every six months

Training compute floating point operations per second (FLOP) versus publication date



Source: Robi Rahman and David Owen, "The training compute of notable AI models has been doubling roughly every six months" (2024) published online at epoch.ai, UBS as of 9 February 2026

As AI clusters demand even larger surface areas for chip integration, Chip-on-Panel-on-Substrate (CoPoS) is emerging as the scalable successor to wafer-based methods. Unlike CoWoS, which is constrained by the circular dimensions of a 300mm silicon wafer, CoPoS utilizes large, rectangular panels—often made of glass or organic materials—to house a significantly higher number of chiplets, those small, specialized chips that perform specific functions, and HBM modules. This transition to panel-level packaging not only improves manufacturing efficiency by reducing material waste at the edges but also allows for the creation of massive "superchips" that would be physically impossible to manufacture on a standard wafer.

While CoWoS and CoPoS focus on internal chip connectivity, Co-Packaged Optics (CPO) addresses the critical bottleneck of external data transmission by bringing fiber-optic signals directly into the chip package. By integrating photonic engines alongside the silicon compute die, CPO eliminates the need for long, power-hungry copper traces that typically carry data to separate transceiver modules. This shift to light-based communication at the package level drastically reduces latency and heat generation, providing the essential bandwidth "highway" needed for next-generation data centers to communicate at speeds of 1.6 terabits and beyond.

Since 2022, total available computing capacity from AI chips across major designers has increased by roughly 3.4x per year (see Fig. 7), supporting the development of increasingly sophisticated models and accelerating broad-based consumer adoption. NVIDIA AI chips currently account for over 60% of total compute, with Google and Amazon comprising much of the remaining share.

Interestingly, while GPUs are central to operations at frontier AI data centers, they account for only about 40% of total power consumption during peak periods. The majority of energy is consumed by power inefficiencies, cooling systems, and interconnects between chips within the data center.

The US currently leads global AI development, primarily owing to its advantages in computational resources and semiconductor innovation. As of 2025, the US accounts for roughly 75% of global GPU cluster performance, with China in second place at around 15% (see Fig. 8).

In the fourth quarter 2025 earnings season, several key companies sharply raised their capex projections (see Fig. 9). Strong demand visibility drove upward revisions to revenue, but this has also required management teams to materially increase capital spending. At the midpoint of their respective guidance ranges, the Big Three internet companies (Alphabet, Meta, and Amazon) guided to capex levels roughly 30% above initial consensus expectations.

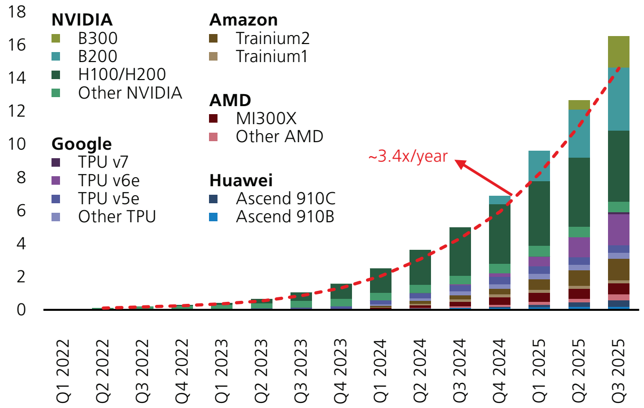
Including Microsoft and Oracle, total capital expenditure for the top five hyperscalers now stands at USD 630bn for calendar year (CY) 2026 and USD 729bn for CY27. This represents upward revisions of 18% and 20%, respectively, versus consensus estimates as of 31 December 2025.

While aggregate revenue and operating cash flow estimates were revised higher, the increase in capex has driven a sharp downward revision to free cash flow (FCF). For the largest AI spenders, consensus FCF expectations are now USD 91bn in 2026 and USD 149bn in 2027—down 49% and 38%,

Figure 7

Global AI computing capacity is doubling every seven months

Cumulative compute capacity, in millions of NVIDIA H-100 equivalent units

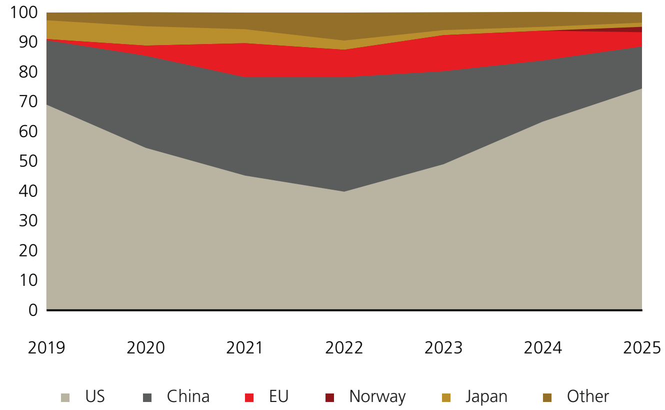


Note: A floating point operation (FLO) refers to the amount of computational work required to train an AI model.
Source: FactSet, UBS as of 9 February 2026

Figure 8

The US hosts the majority of GPU cluster performance

Share of aggregate performance (16-bit FLOP/s), in %



Source: Konstantin F. Pilz et al. "The US hosts the majority of GPU cluster performance, followed by China" (2025) published online at epoch.ai, UBS as of 9 February 2026 respectively, compared with year-end 2025 estimates. Lower expected FCF likely constrains further upside revisions to capital investment and may signal that we are approaching peak spending growth. Meta has also indicated the potential to move to a net debt positive balance sheet, meaning debt could exceed cash, implying that capex may surpass internally generated cash flow. While this outcome is possible, we believe it would likely be constrained by shareholder response and would represent peak capex funding capacity.

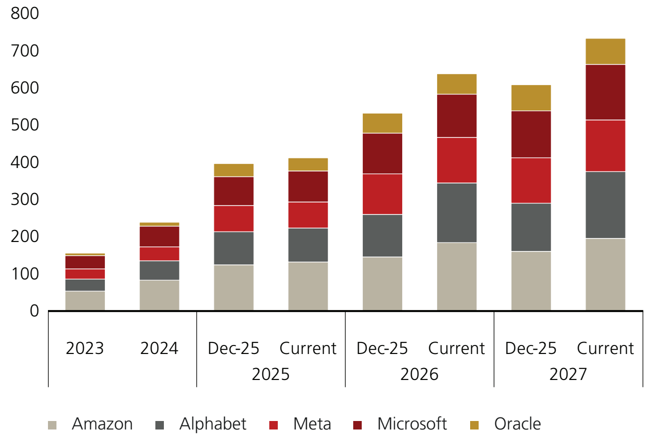
While we acknowledge the risk of a midcycle slowdown in capex buildouts over the next 12-24 months, we believe the medium-term outlook for capex spending remains robust. We estimate total capex could reach USD 1.3 trillion by 2030, implying a 25% compound annual growth rate from 2025 to 2030. To justify this level of investment, productivity gains of roughly USD 6 trillion by 2030, around 10% of today's global labor market, would be required. We view this hurdle as achievable, supported by historical productivity trends and the broad, cross-sector deployment of AI technologies.

Semiconductors sit at the intersection of national security, economic leadership, and technological sovereignty, making the industry a focal point of geopolitical competition. For the US, supply chain fragility and rising tensions have reinforced the priority to regain its technical edge in design and manufacturing. Federal efforts, including incentives under the 2022 CHIPS and Science Act, aim to expand domestic fabrication, fund research, and build a skilled workforce. The strategic objective is to secure access to leading edge technologies and reduce reliance on foreign suppliers, with implications that stretch from commercial AI to defense systems and critical infrastructure edge technologies. The global race is intensified by US export controls on advanced equipment and AI chips, as well as by China's push for self-sufficiency. Leading Chinese firms are developing domestic AI chips and software to cut dependence on foreign technologies, while local chipmakers scale production to meet robust domestic demand. Backed by state-aligned capex, foundries are addressing yield and tooling constraints. Based on recent adoption trends in data center infrastructure, we estimate the localization rate for domestically made GPU chips in mainland China could approach 40% by 2027.

The rise of interconnected deals among leading AI firms evokes echoes of dotcom-era vendor financing, though today's structures and disclosures are far more rigorous. At its peak, vendor financing from North American suppliers exceeded 120% of their pretax earnings, a staggering figure. While vendor financing still plays a role in the market, its scale has diminished. We estimate that NVIDIA's current collaborations represent around 10% of its forecasted pretax earnings for 2026. Even so, the experience of the dotcom era serves as a cautionary tale: Vendor financing remains a potential risk that warrants close monitoring in the coming quarters.

Stepping back, the scale of today's AI infrastructure buildout is unprecedented, on track to become the largest megaproject in human history. What began decades ago with the invention of the microchip has evolved into a global race toward artificial general intelligence (AGI), alongside a shift to a digital asset—or token-based—economy in which AI tokens serve as the fundamental unit of value for computing, data, and intelligence. As AI adoption accelerates, chips will play an increasingly central role, not only in powering this transformation, but also in capturing a growing share of the resulting economic value and productivity gains in the years ahead. Semiconductors, therefore, remain a cornerstone of our *AI* Transformational Innovation Opportunity (TRIO).

Figure 9
Estimates of hyperscaler capex continue to rise
Annual consensus capital expenditures estimates, in USD bn



Source: FactSet, UBS as of 9 February 2026

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